Amendments to the Sp cification

Please amend the paragraph that beings at line 5 of page 19 of the disclosure as follows:

B2

In one embodiment, T-stage 111 translates macroinstructions into ld-alu (load data and perform arithmetic/logical operation on the loaded data) or ld-alu-st (load data, perform arithmetic/logical operation, store result) microinstructions. The generation of ld-alu and ld-alu-st instructions is described in more detail in U.S. Patent 6,338,136 (Docket IDT:1503) entitled, *PAIRING OF LOAD-ALU-STORE WITH CONDITIONAL BRANCH*, having the same assignee, which is hereby incorporated by reference. Ld-alu instructions may be referred to herein as load instructions and ld-alu-st instructions may be referred to herein as load and/or store instructions in that they load data from or store data to memory or I/O device 194.

Please amend the paragraph that begins at line 4 of page 22 of the disclosure as follows:

B3

As shown, data is provided to operand registers 168 from three sources: data unit 144, a result forwarding cache (RFC) 166, and directly from execution units 164 via signal 167. Operation of the RFC is completely described in U.S. Patent 6,343,359 (Docket CNTR:1501) entitled "RESULT FORWARDING CACHE", assigned to a common assignee, which is hereby incorporated by reference. Multiplexers 154 operate to select one of the three data sources for providing operands to operand registers 168 as controlled by compare logic 156. Compare logic 156 compares virtual address 143 with virtual addresses 153, 163, 173 and 183 and controls multiplexers 154 via control signal 155 based on whether a storehit occurred between the G-stage 151 load instruction and any store instructions present in the E-stage 161, S-stage 171 or W-stage 181, based on the virtual address comparison. The control of multiplexers 154 is described below in more detail with respect to Figure 3.

Please amend the paragraph that begins at line 11 of page 34 of the disclosure as follows:

B4

Stalling the pipeline 100 allows the stages below the E-stage 161 to drain all store results in the pipeline 100, in step 412. In particular, store results in the S-stage 171, W-stage 181 and store buffers 188 are written to data cache 242 of Figure 2. After all the store results in pipeline 100 are drained, the load instruction causing the storehit and virtual aliasing condition is reissued within the data unit 144, in step 412. How data unit 144 reissues instructions is described in more detail in U.S. Patent 6,549,985 (Docket IDT:1566), entitled *METHOD AND APPARATUS FOR RESOLVING ADDITIONAL LOAD MISSES AND PAGE TABLE WALKS UNDER ORTHOGONAL STALLS IN A SINGLE PIPELINE PROCESSOR*, having the same assignee, which is hereby incorporated by reference. Because no storehits will occur in the pipeline 100 upon reissue of the load instruction due to the draining of the pipeline 100, compare logic 156 will select data unit 144, and control logic 218 will control multiplexers 252 and 256 to select data from data cache 242, in step 412.

Please amend the paragraph that begins at line 11 of page 36 of the disclosure as follows:

B5

If no access to a non-cacheable region is detected, control logic 218 determines whether a virtual storehit was detected in the E-stage 161, S-stage 171 or W-stage 181, based upon a virtual address comparison as indicated by signal virt_match 159, in step 406. If a virtual storehit was detected, then compare logic 156 will not select data from data unit 144, but instead will select data forwarded directly from the E-stage 161 or from the RFC 166, in step 416.